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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/502,460	09/07/2004	Axel Hulsmann	08788.0037USWO	3738
23552	7590	08/10/2006	EXAMINER	
MERCHANT & GOULD PC P.O. BOX 2903 MINNEAPOLIS, MN 55402-0903			NGUYEN, THINH T	
			ART UNIT	PAPER NUMBER
			2818	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/502,460

Applicant(s)

HULSMANN, AXEL

Examiner

Thinh T. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 July 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED OFFICE ACTION

1. Applicant's election of claims 1-10 (Species III), read on fig 3, in the communication with the Office on 6/12/2006 is acknowledged.

Specification

2. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.
3. The specification is objected to for the use of Acronym HLS (page 6 line 11) and acronym HZLS (page 6 line 21). Since the Applicant does provide any explanations for these acronyms, it is not possible for a person skilled in the art to understand what these acronyms mean.

Clarification is required.

Drawings

4. The drawings (fig 1, fig 2, and fig 3) are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: layers 1,2,3,4,5,6,7,8,9,10,11. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any

amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. The drawing is objected to for the use of labels HLS and HLZS in fig 1, fig 2, and fig 3. Since the Applicant does provide any explanations for these acronyms, it is not possible for a person skilled in the art to understand what these acronyms mean.

Clarification is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b) that form the basis for the rejections under this section made in this office action.

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 1-2,4, 6, 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Katoh (U.S. Patent 5,041,882).

REGARDING CLAIM 1

Katoh discloses (in fig 1, fig 4, column 1 line 6-67, particularly line 6-12 and line 44-49) a heterobipolar transistor (column 3 lines 20-30), comprising an emitter which includes a first semiconductor layer (fig 1 layer 9," made of a first semiconductor material and a second semiconductor layer (fig 1 layer 7) made of a second semiconductor material, a band gap value of the first semiconductor material being smaller than a band gap value of the second semiconductor material, characterized in that a semiconductor intermediate layer (fig 1 layer 8) made of an intermediate layer semiconductor material is disposed between the first semiconductor layer and the second semiconductor layer (and that a band gap value of the intermediate layer semiconductor material is greater than the band gap value of the first semiconductor material and smaller than the band gap value of the second semiconductor material.(column 3 lines 20-30) .

Noted that Katoh discloses a plurality of layer with band-gap gradually smaller from emitter to base therefore correctly anticipated claim 1(column 1 lines 6-12 and 44-49, column 3 lines 20-30).

REGARDING CLAIM 2

Katoh discloses a heterobipolar transistor characterized in that the intermediate layer semiconductor material is lattice adapted (Katoh reference column 3 lines 24-26) to the first semiconductor material and/or the second semiconductor material.

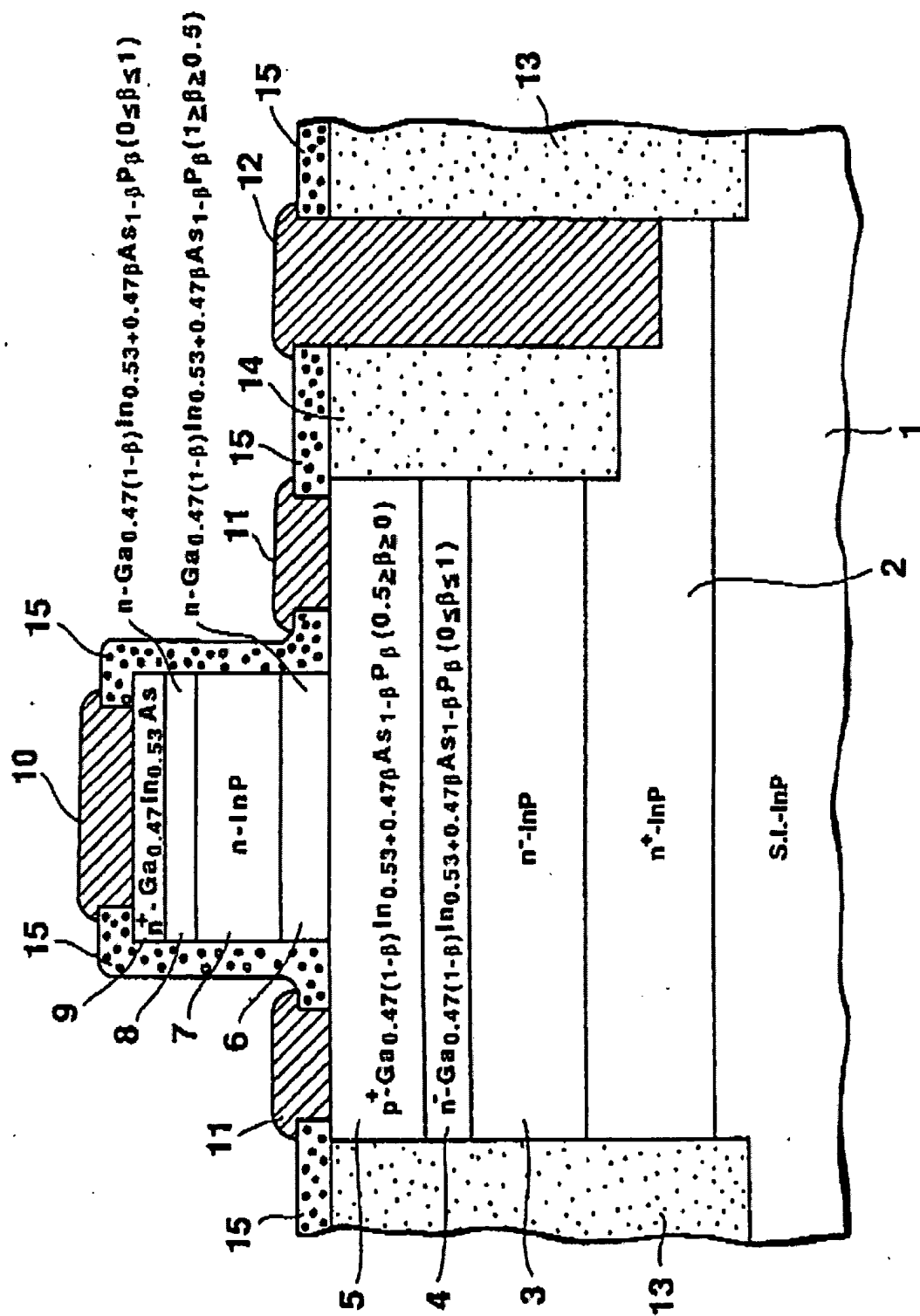


FIG. 1

REGARDING CLAIM 4

Katoh discloses a heterobipolar transistor, characterized in that the first semiconductor material comprises InGaAs (Katoh fig 1 layer 9, "GaInAs"), the second semiconductor material comprises InP (Katoh fig 1 layer 7), and the intermediate layer semiconductor material comprises InGaAsP (Katoh fig 1 layer 8, "GaInAsP").

REGARDING CLAIM 6

Katoh discloses a heterobipolar transistor, characterized in that a sequence of n ($n \geq 2$) stacked semiconductor intermediate layers constituted by the semiconductor intermediate layer and at least one other semiconductor layer made of another intermediate layer semiconductor material are disposed between the first semiconductor layer (Katoh fig 1 layer 9) and the second semiconductor layer (Katoh fig 1 layer 7, or 6 or 7/6), that the at least one other semiconductor layer is disposed between the semiconductor intermediate layer (Katoh fig 1 layer 8, or 7 or 8/7) and the second semiconductor layer and that a band gap value of the other intermediate layer semiconductor material is greater than the band gap value of the Intermediate layer semiconductor material and smaller than the band gap value of the second semiconductor material.

Noted that Katoh discloses a plurality of layer with band-gap gradually smaller from emitter to base therefore correctly anticipated claim 1 (column 1 lines 6-12 and 44-49, column 3 lines 20-30).

REGARDING CLAIM 9

Katoh discloses a heterobipolar transistor characterized in that the first semiconductor layer is contacted metallicity. Noted that layer 9 in fig 1 of Katoh reference corresponds to first

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semiconductor layer 9 PCT document of the applicant and is metallically contacted with layer 10. which is made with gold (Au) (see Katoh reference column 7 line 47) and gold is metal.

Claim Rejections - 35 USC § 103

8. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 3,5,7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh (U.S. Patent 5,041,882).

REGARDING CLAIM 3

With regard to claim 3, as set forth in the rejection of claim 1, Katoh discloses all the invention except for disclosing the limitation “ the band gap value of the intermediate layer semiconductor material equals half the sum of the band gap value of the first semiconductor material plus the band gap value of the second semiconductor material.”--.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate this feature into the Katoh device and come up with the invention of claim 3 since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum value or workable range involves only routine skills in the art

(in this case the intermediate layer band gap optimum value and averaging algorithm with graded increase that can be discovered by a person of ordinary skill in the art using computer simulation and optimization or regular experiment)

REGARDING CLAIM 5

With regard to claim 5, as set forth in the rejection of claim 1, Katoh discloses all the invention of claim 5 except for using InAlAs for the second material and AlGaInAs for the intermediate layer. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate this feature into the Katoh device and come up with the invention of claim 5 since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended purpose.

REGARDING CLAIM 7

With regard to claim 7, as set forth in the rejection of claim 6, Katoh discloses all the invention except for the limitation wherein the first semiconductor material has a band gap value B_e , the second semiconductor material has a band gap value B_z , and an intermediate layer semiconductor material of a j .sup.th of the n semiconductor intermediate layers ($2 \leq j \leq n$) has a band gap value B_j , where $B_j = B_e + j + (1/(1+n))(B_z - B_e)$.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate this feature into the Katoh Device and come up with the invention of claim 7. since it has been held that where the general conditions of a claim are disclosed in the prior art discovering the optimum value or workable range involves only routine skills in the art.

In this case the intermediate layer j band gap B_j with B_e as the band gap of the first semiconductor layer using optimization and averaging formula with graded increase that can be

discovered by a person of ordinary skill in the art using computer simulation and optimization or regular experiment at the time the invention was made . Noted that Applicant formula for specifying the band gap B_j of the intermediate layer j is just a simple algorithm for averaging the band gap of the intermediate layer.

10. Claims 8,10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh (U.S. Patent 5,041,882) in view of Schetzina (US patent 5,679,965).

REGARDING CLAIM 8

With regard to claim 8, as set forth in the rejection of claim 6 and 7, Katoh discloses all the invention except for the limitations characterized in that the number n of the semiconductor intermediate layers (31, 32, 33) constituting the sequence is selected such that a quasi linear transition is obtained between the band gap value of the first semiconductor material and the band gap value of the second semiconductor material due to the band gap values of the intermediate layer semiconductor materials disposed between the first semiconductor material and the second semiconductor material . Schetzina, however, discloses (in column 8 line 54-59,fig 26,fig 27A,fig 27B) a plurality of stepped graded layers (continuously increasing or decreasing) .

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate this feature, as taught by Schetzina, into the Katoh device and come up with the invention of claim 8 since both Katoh and Schetzina are in the same field of endeavor of fabricating heterojunction bipolar transistor (see Katoh reference column 1 line 14 and Schetzina reference column 11 lines 41-42). Also noted that stepped graded layers are quasi-linear.

REGARDING CLAIM 10

Katoh discloses (in fig 1, column 1 line 6) a heterobipolar transistor characterized in that a further semiconductor layer (Katoh layer 6 fig. 1), borders on the second semiconductor layer 5, at a side remote from the semiconductor intermediate layers (layers 7,8 fig 1) and that the further semiconductor layer (Katoh fig 1 layer 6) borders on a base (5).

the rationale as why claim 8 is obvious over Katoh in view of Schetzina has been set forth in the rejection of claim 8.

11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

12. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

13. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

CONCLUSION

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:30am-6: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached at 571-272-1907.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thinh T. Nguyen



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